

AUIRFR9024N AUIRFU9024N

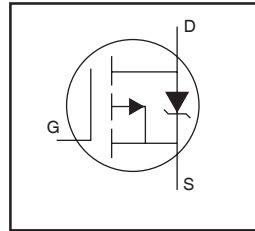
Features

- Advanced Planar Technology
- Low On-Resistance
- P-Channel
- Dynamic dV/dT Rating
- 150°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified *

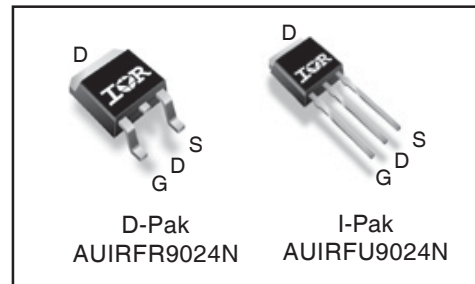
Description

Specifically designed for Automotive applications, this Cellular design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve low on-resistance per silicon area. This benefit combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in Automotive and a wide variety of other applications.

HEXFET® Power MOSFET



| | |
|-------------------|---------------|
| $V_{(BR)DSS}$ | -55V |
| $R_{DS(on)}$ max. | 0.175Ω |
| I_D | -11A |



| | | |
|----------|----------|----------|
| G | D | S |
| Gate | Drain | Source |

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

| | Parameter | Max. | Units |
|---------------------------------|---|------------------------|-------|
| $I_D @ T_C = 25^\circ\text{C}$ | Continuous Drain Current, $V_{GS} @ -10\text{V}$ | -11 | A |
| $I_D @ T_C = 100^\circ\text{C}$ | Continuous Drain Current, $V_{GS} @ -10\text{V}$ | -8 | |
| I_{DM} | Pulsed Drain Current ① | -44 | |
| $P_D @ T_C = 25^\circ\text{C}$ | Power Dissipation | 38 | W |
| | Linear Derating Factor | 0.30 | W/°C |
| V_{GS} | Gate-to-Source Voltage | ± 20 | V |
| E_{AS} | Single Pulse Avalanche Energy (Thermally limited) ② | 62 | mJ |
| I_{AR} | Avalanche Current ① | -6.6 | A |
| E_{AR} | Repetitive Avalanche Energy ① | 3.8 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ③ | -10 | V/ns |
| T_J | Operating Junction and | -55 to + 150 | °C |
| T_{STG} | Storage Temperature Range | | |
| | Soldering Temperature, for 10 seconds | 300 (1.6mm from case) | |

Thermal Resistance

| | Parameter | Typ. | Max. | Units |
|-----------------|------------------------------------|------|------|-------|
| $R_{\theta JC}$ | Junction-to-Case | — | 3.3 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient (PCB mount) ** | — | 50 | |
| $R_{\theta JA}$ | Junction-to-Ambient | — | 110 | |

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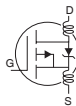
*Qualification standards can be found at <http://www.irf.com/>

Static Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---------------------------------|--------------------------------------|------|-------|-------|----------|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | -55 | — | — | V | $V_{GS} = 0V, I_D = -250\mu A$ |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | -0.05 | — | V/°C | Reference to $25^\circ\text{C}, I_D = -1\text{mA}$ |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | — | 0.175 | Ω | $V_{GS} = -10V, I_D = -6.6A$ ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | -2.0 | — | -4.0 | V | $V_{DS} = V_{GS}, I_D = -250\mu A$ |
| gfs | Forward Transconductance | 2.5 | — | — | S | $V_{DS} = -25V, I_D = -7.2A$ ⑥ |
| I_{DSS} | Drain-to-Source Leakage Current | — | — | -25 | μA | $V_{DS} = -55V, V_{GS} = 0V$ |
| | | — | — | -250 | | $V_{DS} = -44V, V_{GS} = 0V, T_J = 150^\circ\text{C}$ |
| I_{GSS} | Gate-to-Source Forward Leakage | — | — | 100 | nA | $V_{GS} = -20V$ |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | $V_{GS} = 20V$ |

Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

| | | | | | | |
|--------------|---------------------------------|---|-----|-----|----|---|
| Q_g | Total Gate Charge | — | — | 19 | nC | $I_D = -7.2A$ $V_{DS} = -44V$ $V_{GS} = -10V$, See Fig 6 and 13 ④⑥ |
| Q_{gs} | Gate-to-Source Charge | — | — | 5.1 | | |
| Q_{gd} | Gate-to-Drain ("Miller") Charge | — | — | 10 | | |
| $t_{d(on)}$ | Turn-On Delay Time | — | 13 | — | ns | $V_{DD} = -28V$ $I_D = -7.2A$ $R_G = 24\ \Omega$ $R_D = 3.7\ \Omega$, See Fig.10 ④⑥ |
| t_r | Rise Time | — | 55 | — | | |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 23 | — | | |
| t_f | Fall Time | — | 37 | — | | |
| L_D | Internal Drain Inductance | — | 4.5 | — | nH | Between lead, 6mm (0.25in.) from package and center of die contact |
| L_S | Internal Source Inductance | — | 7.5 | — | | |
| C_{iss} | Input Capacitance | — | 350 | — | pF | $V_{GS} = 0V$ $V_{DS} = -25V$ $f = 1.0\text{MHz}$, see Fig.5 ⑥ |
| C_{oss} | Output Capacitance | — | 170 | — | | |
| C_{rss} | Reverse Transfer Capacitance | — | 92 | — | | |



Diode Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|----------|---|---|------|------|-------|---|
| I_S | Continuous Source Current (Body Diode) | — | — | -11 | A | MOSFET symbol showing the integral reverse p-n junction diode. |
| I_{SM} | Pulsed Source Current (Body Diode) ① | — | — | -44 | | |
| V_{SD} | Diode Forward Voltage | — | — | -1.6 | V | $T_J = 25^\circ\text{C}, I_S = -7.2A, V_{GS} = 0V$ ④ |
| t_{rr} | Reverse Recovery Time | — | 47 | 71 | ns | $T_J = 25^\circ\text{C}, I_F = -7.2A$ |
| Q_{rr} | Reverse Recovery Charge | — | 84 | 130 | nC | $di/dt = 100A/\mu s$ ④⑥ |
| t_{on} | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D) | | | | |



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Starting $T_J = 25^\circ\text{C}, L = 2.8\text{mH}$
 $R_G = 25\ \Omega, I_{AS} = -6.6A$ (See Figure 12)
- ③ $I_{SD} \leq -6.6A, di/dt \leq -240A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$

- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ This is applied for I-PAK, L_S of D-PAK is measured between lead and center of die contact.
- ⑥ Uses IRF9Z24N data and test conditions.

** When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

Qualification Information[†]

| | | | |
|-----------------------------------|----------------------|---|------|
| Qualification Level | | Automotive (per AEC-Q101) ^{††} | |
| | | Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level. | |
| Moisture Sensitivity Level | | D PAK | MSL1 |
| | | I-PAK | N/A |
| ESD | Machine Model | Class M2(+/-150V) ^{†††} AEC-Q101-002 | |
| | Human Body Model | Class H1A(+/-500V) ^{†††} AEC-Q101-001 | |
| | Charged Device Model | Class C5(+/-2000V) ^{†††} AEC-Q101-005 | |
| RoHS Compliant | | Yes | |

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/>

†† Exceptions to AEC-Q101 requirements are noted in the qualification report.

††† Highest passing voltage

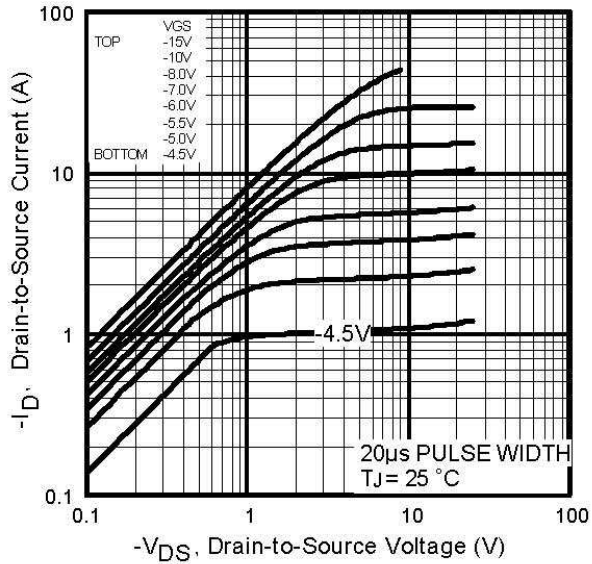


Fig 1. Typical Output Characteristics

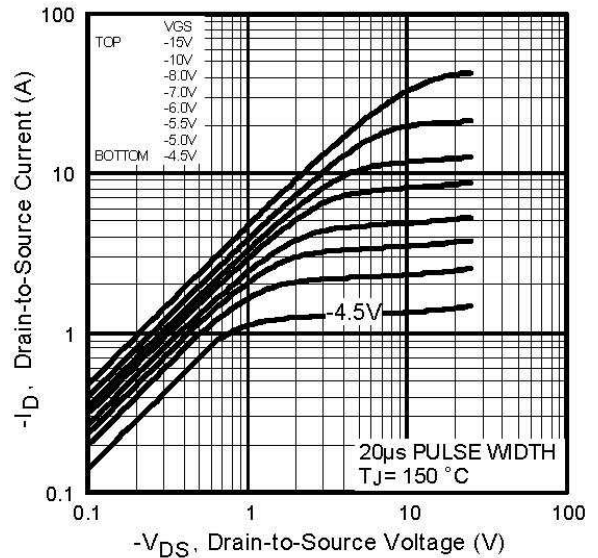


Fig 2. Typical Output Characteristics

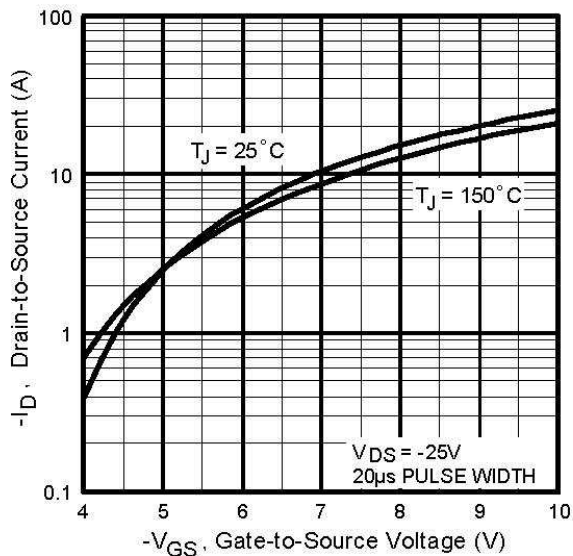


Fig 3. Typical Transfer Characteristics

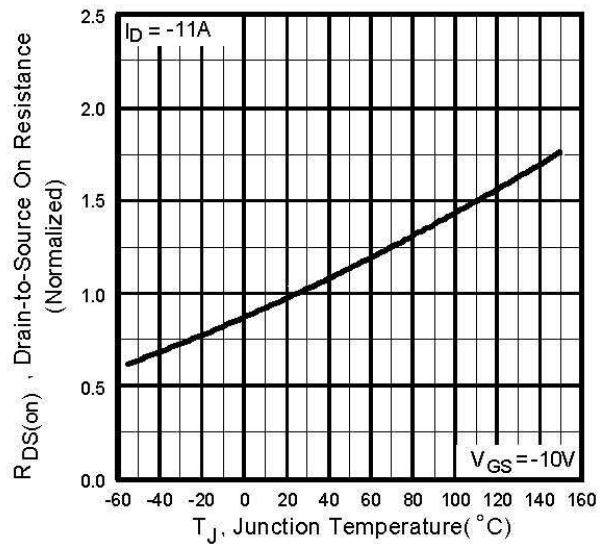


Fig 4. Normalized On-Resistance Vs. Temperature

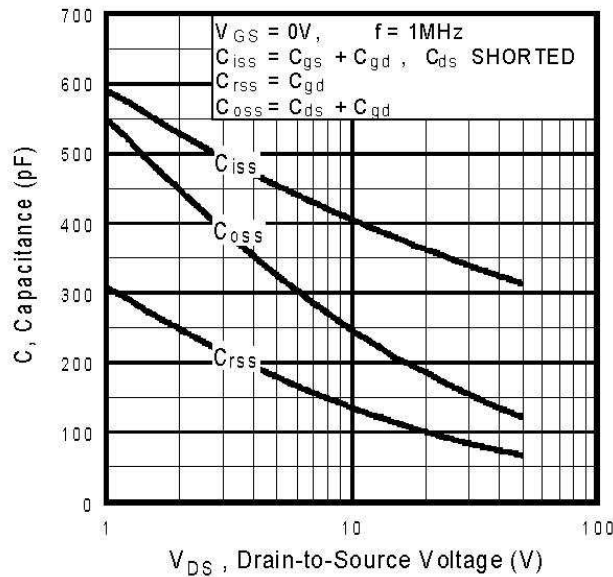


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

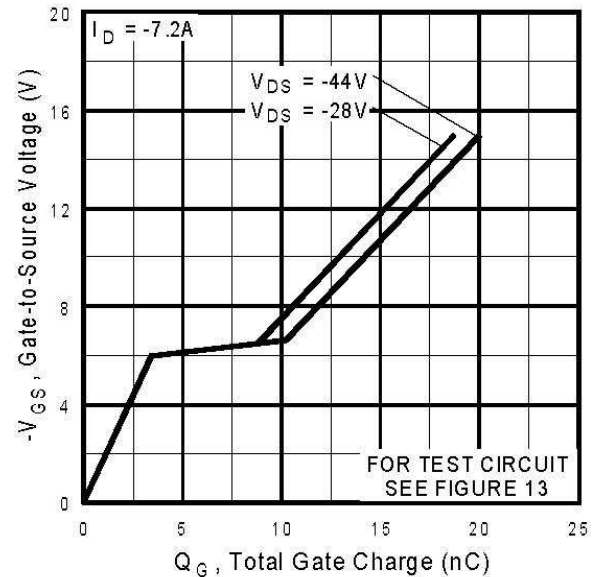


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

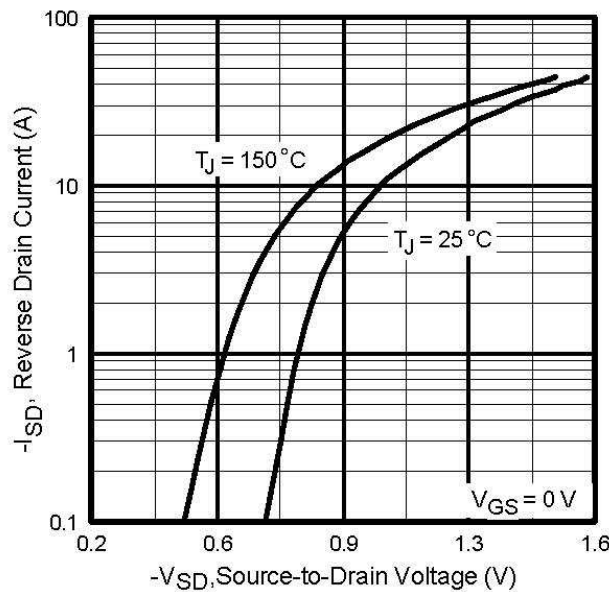


Fig 7. Typical Source-Drain Diode Forward Voltage

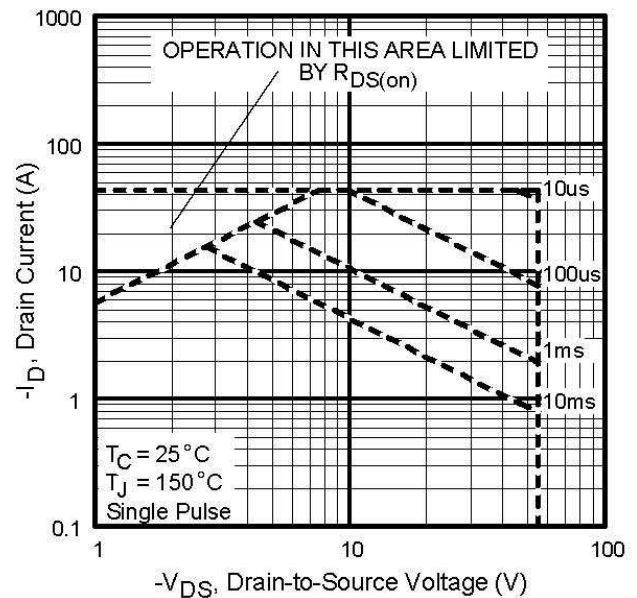


Fig 8. Maximum Safe Operating Area

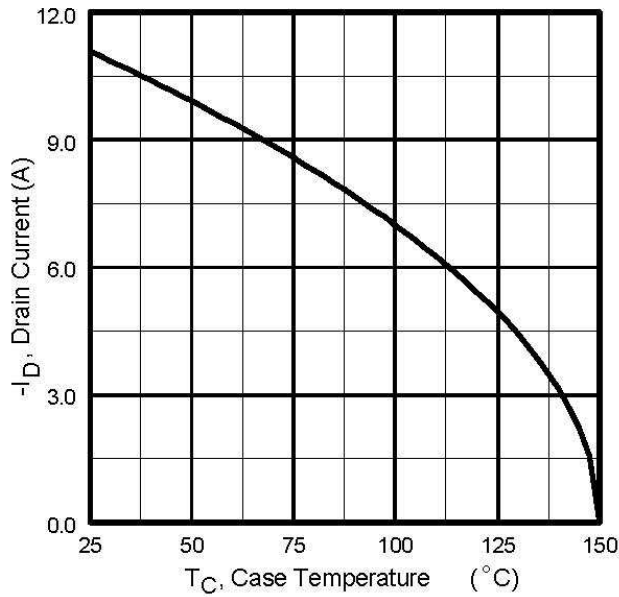


Fig 9. Maximum Drain Current Vs. Case Temperature

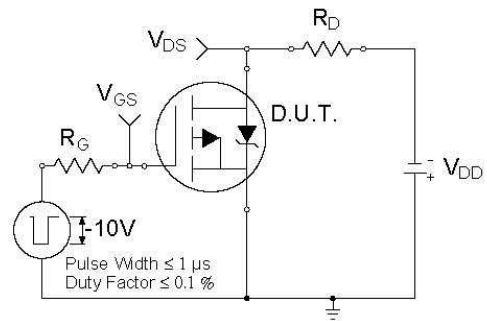


Fig 10a. Switching Time Test Circuit

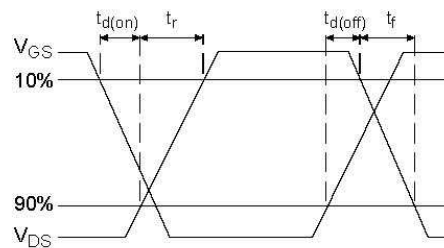


Fig 10b. Switching Time Waveforms

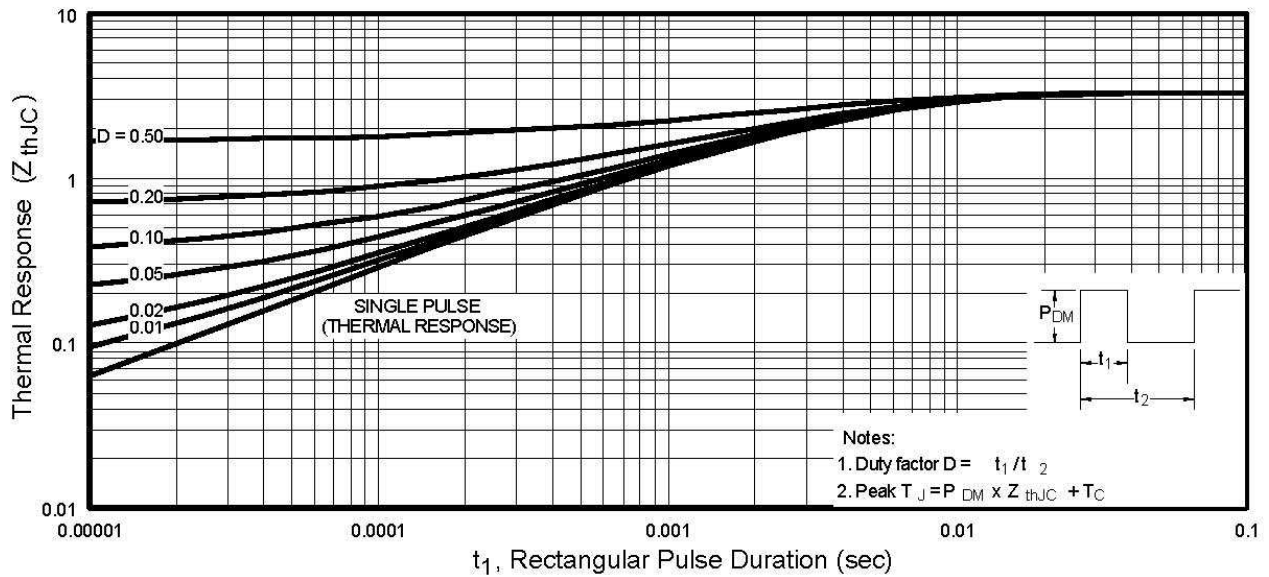


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

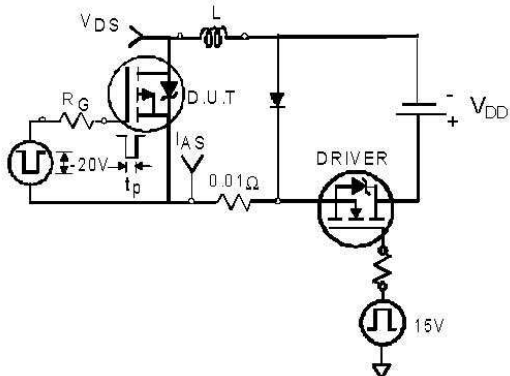


Fig 12a. Unclamped Inductive Test Circuit

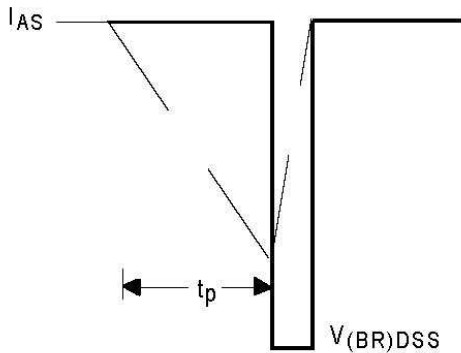


Fig 12b. Unclamped Inductive Waveforms

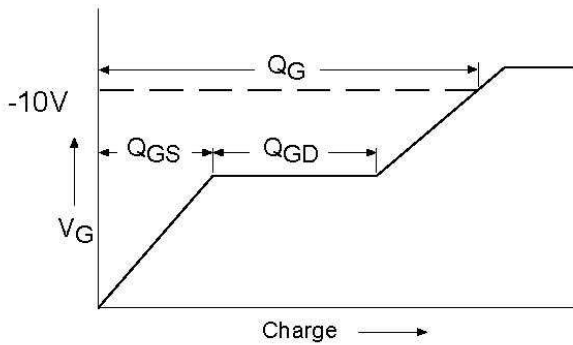


Fig 13a. Basic Gate Charge Waveform

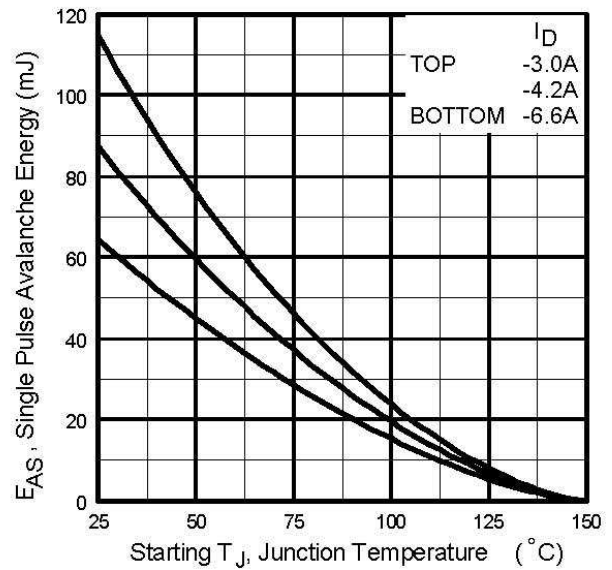


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

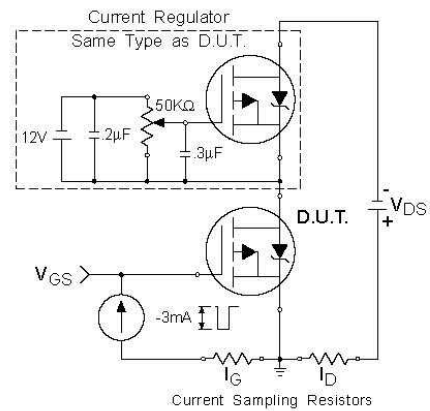
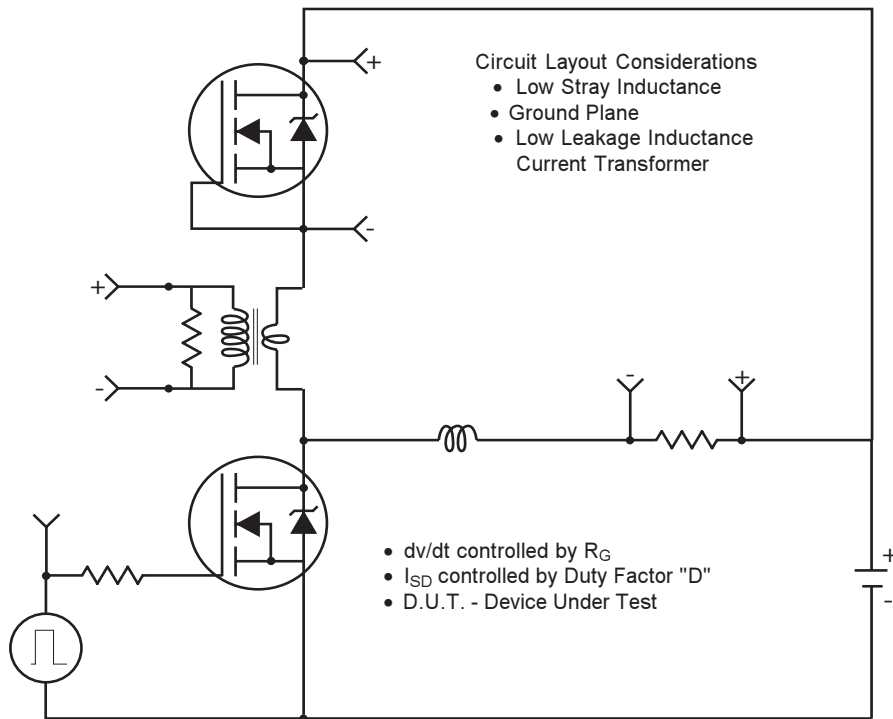


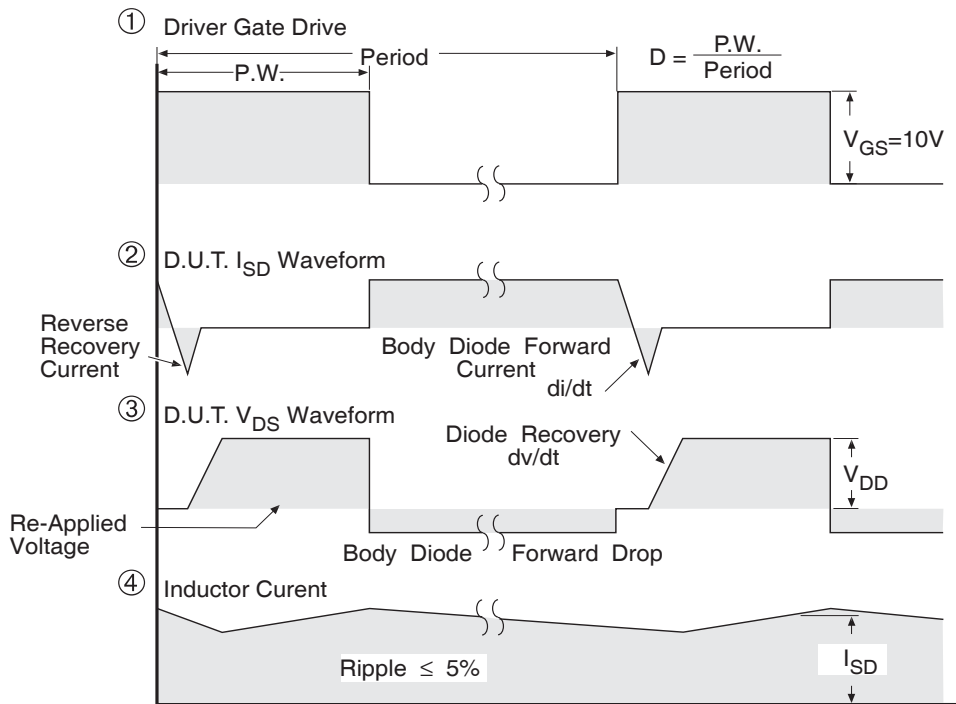
Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel

** Use P-Channel Driver for P-Channel Measurements

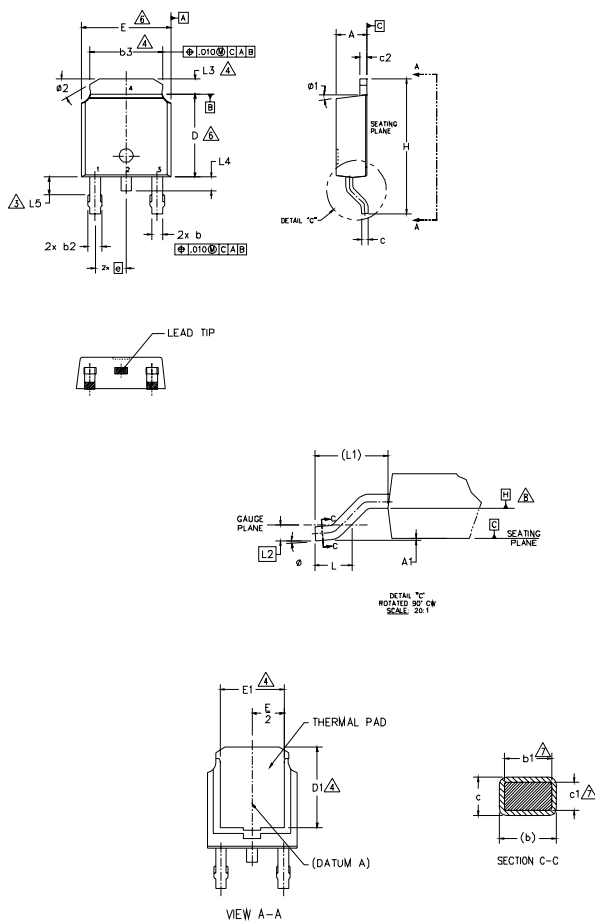


*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 14 For P Channel HEXFETS

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS]
- 3.- LEAD DIMENSION UNCONTROLLED IN L5.
- 4.- DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
- 6.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- 7.- DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
- 8.- DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

| SYMBOL | DIMENSIONS | | | | NOTES |
|--------|-------------|-------|-----------|------|-------|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 2.18 | 2.39 | .086 | .094 | |
| A1 | - | 0.13 | - | .005 | |
| b | 0.64 | 0.89 | .025 | .035 | |
| b1 | 0.65 | 0.79 | .025 | .031 | 7 |
| b2 | 0.76 | 1.14 | .030 | .045 | |
| b3 | 4.95 | 5.46 | .195 | .215 | 4 |
| c | 0.46 | 0.61 | .018 | .024 | |
| c1 | 0.41 | 0.56 | .016 | .022 | 7 |
| c2 | 0.46 | 0.89 | .018 | .035 | |
| D | 5.97 | 6.22 | .235 | .245 | 6 |
| D1 | 5.21 | - | .205 | - | 4 |
| E | 6.35 | 6.73 | .250 | .265 | 6 |
| E1 | 4.32 | - | .170 | - | 4 |
| e | 2.29 BSC | | .090 BSC | | |
| H | 9.40 | 10.41 | .370 | .410 | |
| L | 1.40 | 1.78 | .055 | .070 | |
| L1 | 2.74 BSC | | .108 REF. | | |
| L2 | 0.51 BSC | | .020 BSC | | |
| L3 | 0.89 | 1.27 | .035 | .050 | 4 |
| L4 | - | 1.02 | - | .040 | |
| L5 | 1.14 | 1.52 | .045 | .060 | 3 |
| ø | 0" | 10" | 0" | 10" | |
| ø1 | 0" | 15" | 0" | 15" | |
| ø2 | 25" | 35" | 25" | 35" | |

LEAD ASSIGNMENTS

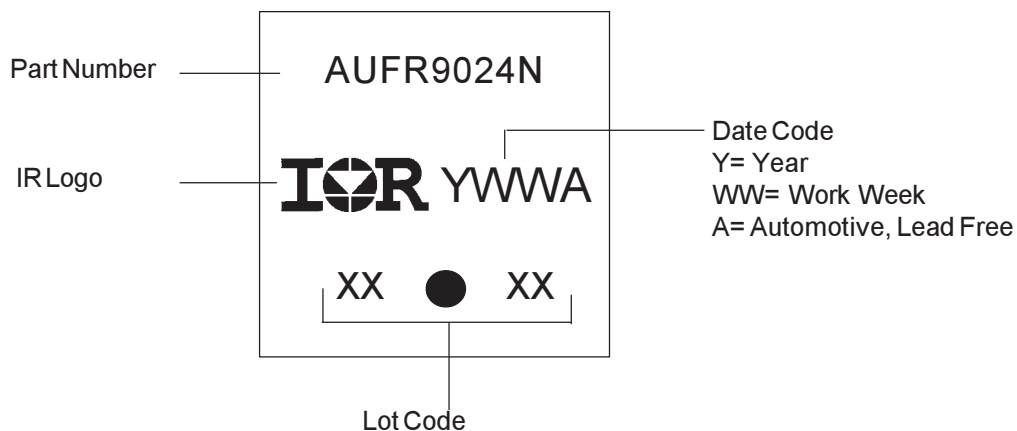
HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBT & CoPAK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

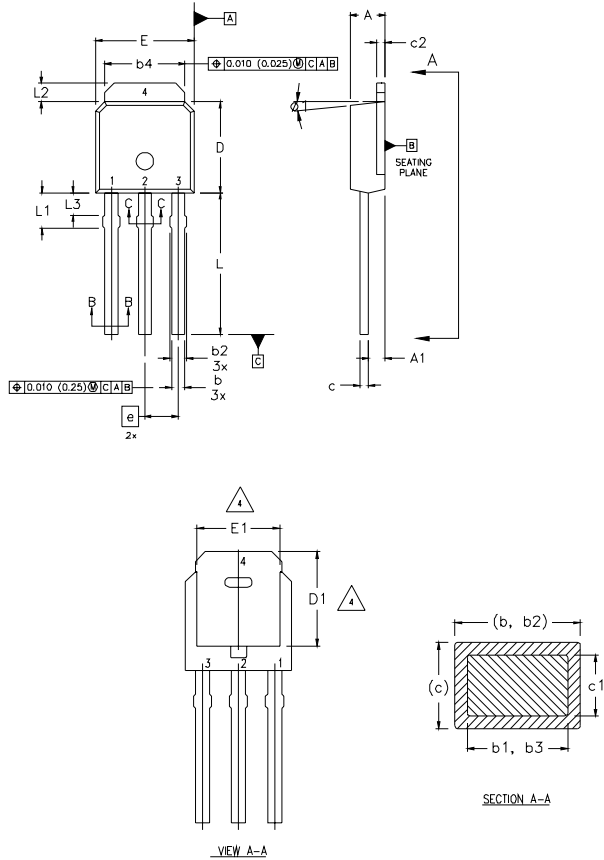
D-Pak (TO-252AA) Part Marking Information



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

www.irf.com

I-Pak (TO-251AA) Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
- 2 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 4 THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
- 5 LEAD DIMENSION UNCONTROLLED IN L3.
- 6 DIMENSION b1, b3 APPLY TO BASE METAL ONLY.
- 7 OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
- 8 CONTROLLING DIMENSION : INCHES.

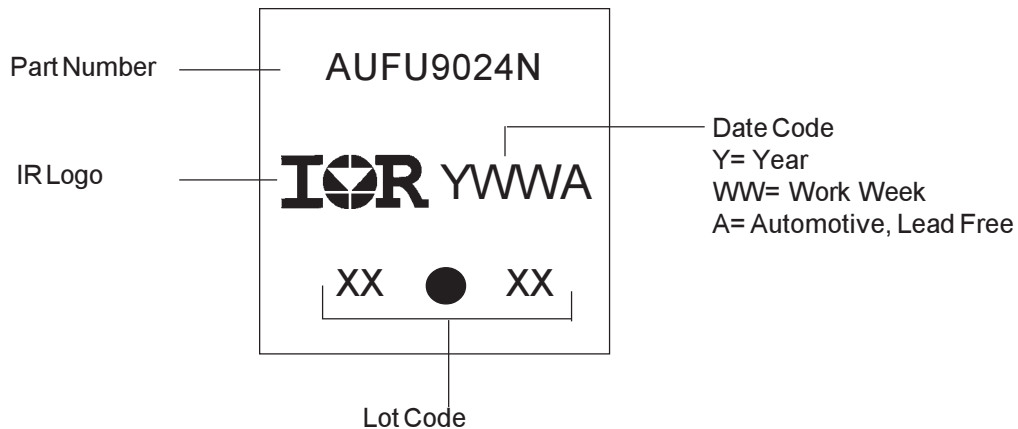
LEAD ASSIGNMENTS

HEXFEEET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

| SYMBOL | DIMENSIONS | | | | NOTES |
|--------|-------------|------|-----------|-------|-------|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 2.18 | 2.39 | 0.086 | .094 | |
| A1 | 0.89 | 1.14 | 0.035 | 0.045 | |
| b | 0.64 | 0.89 | 0.025 | 0.035 | |
| b1 | 0.64 | 0.79 | 0.025 | 0.031 | 4 |
| b2 | 0.76 | 1.14 | 0.030 | 0.045 | |
| b3 | 0.76 | 1.04 | 0.030 | 0.041 | |
| b4 | 5.00 | 5.46 | 0.195 | 0.215 | 4 |
| c | 0.46 | 0.61 | 0.018 | 0.024 | |
| c1 | 0.41 | 0.56 | 0.016 | 0.022 | |
| c2 | .046 | 0.86 | 0.018 | 0.035 | |
| D | 5.97 | 6.22 | 0.235 | 0.245 | 3, 4 |
| D1 | 5.21 | - | 0.205 | - | 4 |
| E | 6.35 | 6.73 | 0.250 | 0.265 | 3, 4 |
| E1 | 4.32 | - | 0.170 | - | 4 |
| e | 2.29 | | 0.090 BSC | | |
| L | 8.89 | 9.60 | 0.350 | 0.380 | |
| L1 | 1.91 | 2.29 | 0.075 | 0.090 | |
| L2 | 0.89 | 1.27 | 0.035 | 0.050 | 4 |
| L3 | 1.14 | 1.52 | 0.045 | 0.060 | 5 |
| ø1 | ø | 15' | ø | 15' | |

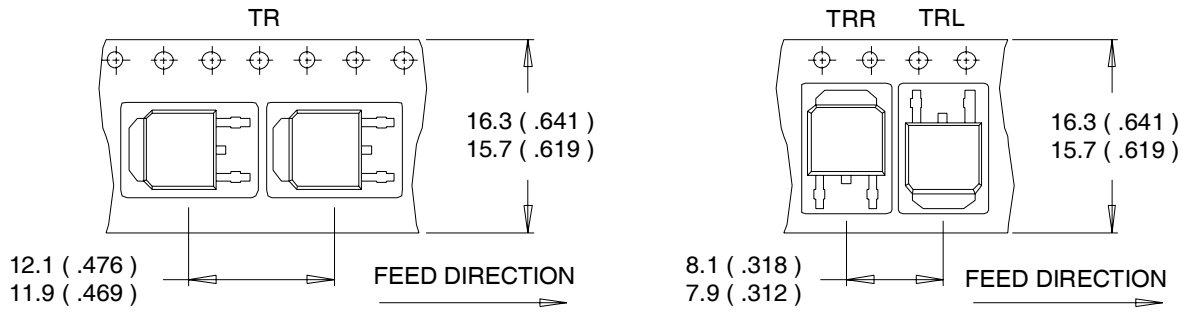
I-Pak (TO-251AA) Part Marking Information



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

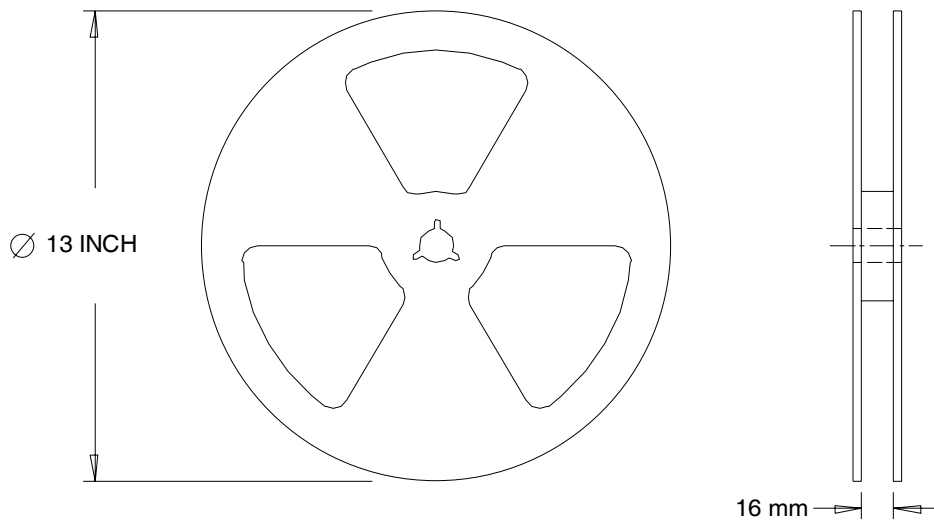
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Ordering Information

| Base part | Package Type | Standard Pack | | Complete Part Number |
|-------------|--------------|---------------------|----------|----------------------|
| | | Form | Quantity | |
| AUIRFR9024N | DPak | Tube | 75 | AUIRFR9024N |
| | | Tape and Reel | 2000 | AUIRFR9024NTR |
| | | Tape and Reel Left | 3000 | AUIRFR9024NTRL |
| | | Tape and Reel Right | 3000 | AUIRFR9024NTRR |
| AUIRFU9024N | IPak | Tube | 75 | AUIRFU9024N |

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For technical support, please contact IR's Technical Assistance Center
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